

Lecture 12

Introduction to Tiled Chip Multicore Processors



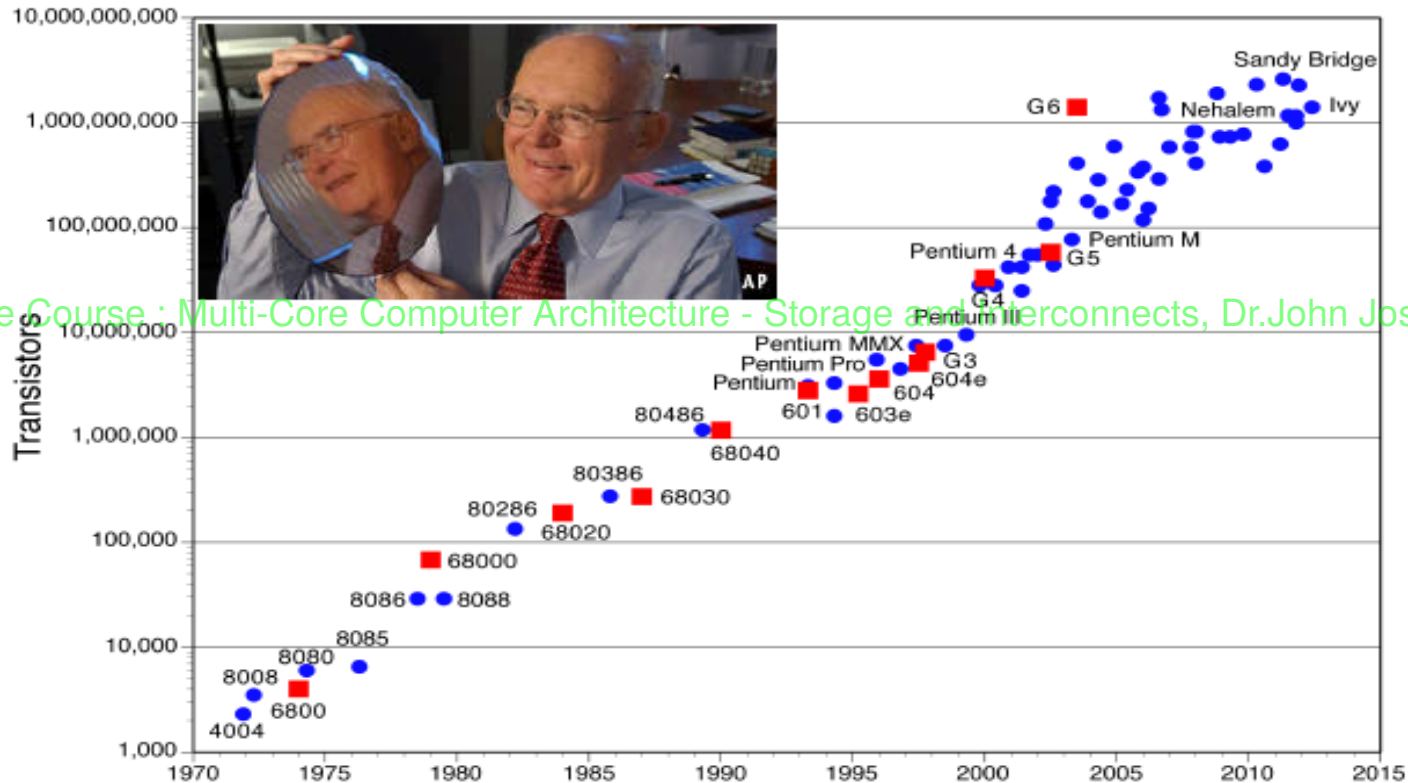
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Dr. John Jose

Assistant Professor

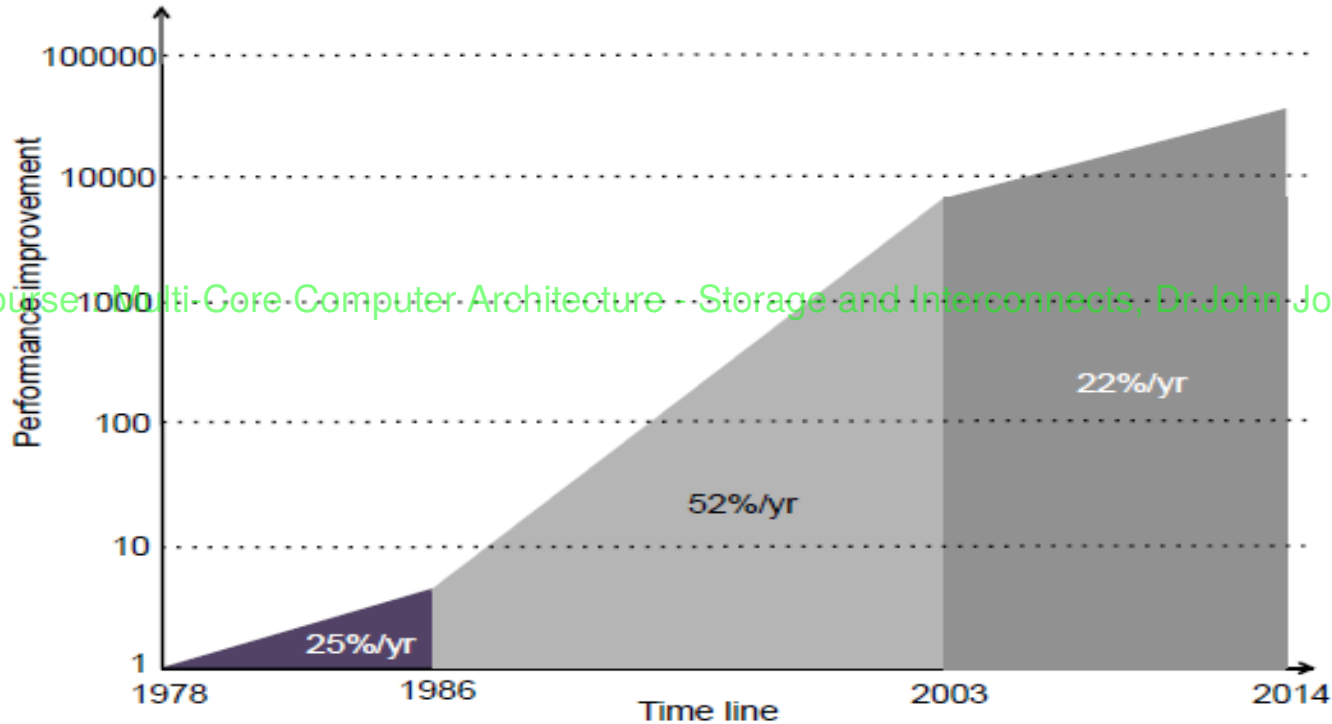
**Department of Computer Science & Engineering
Indian Institute of Technology Guwahati, Assam.**

Impact of VLSI in processor trends



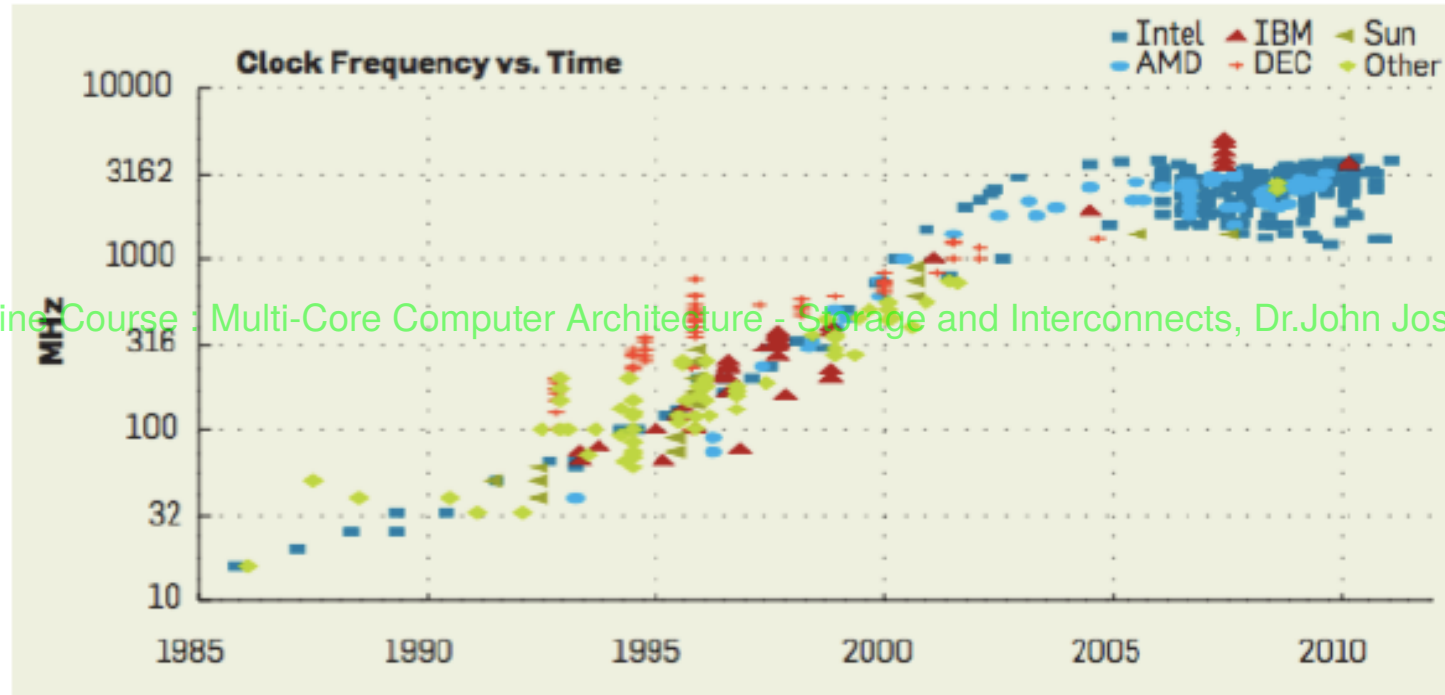
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Processors Performance



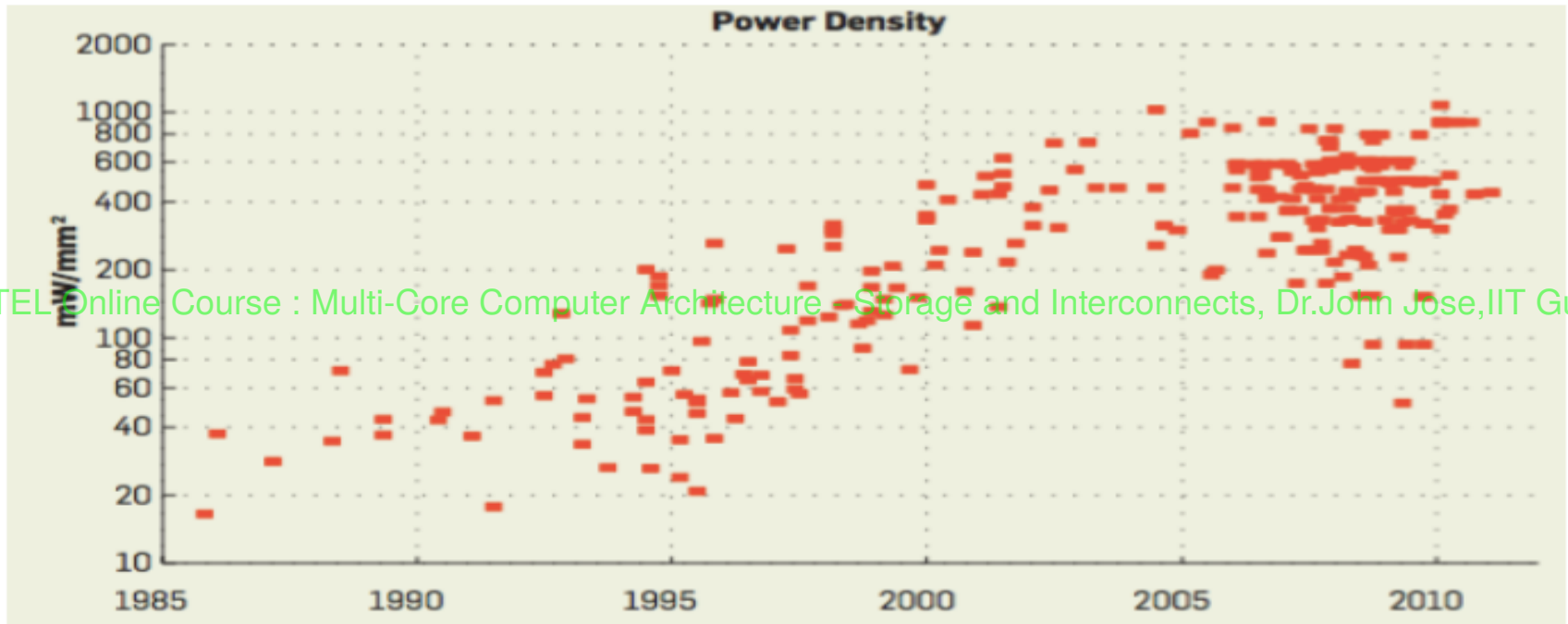
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Frequency Wall



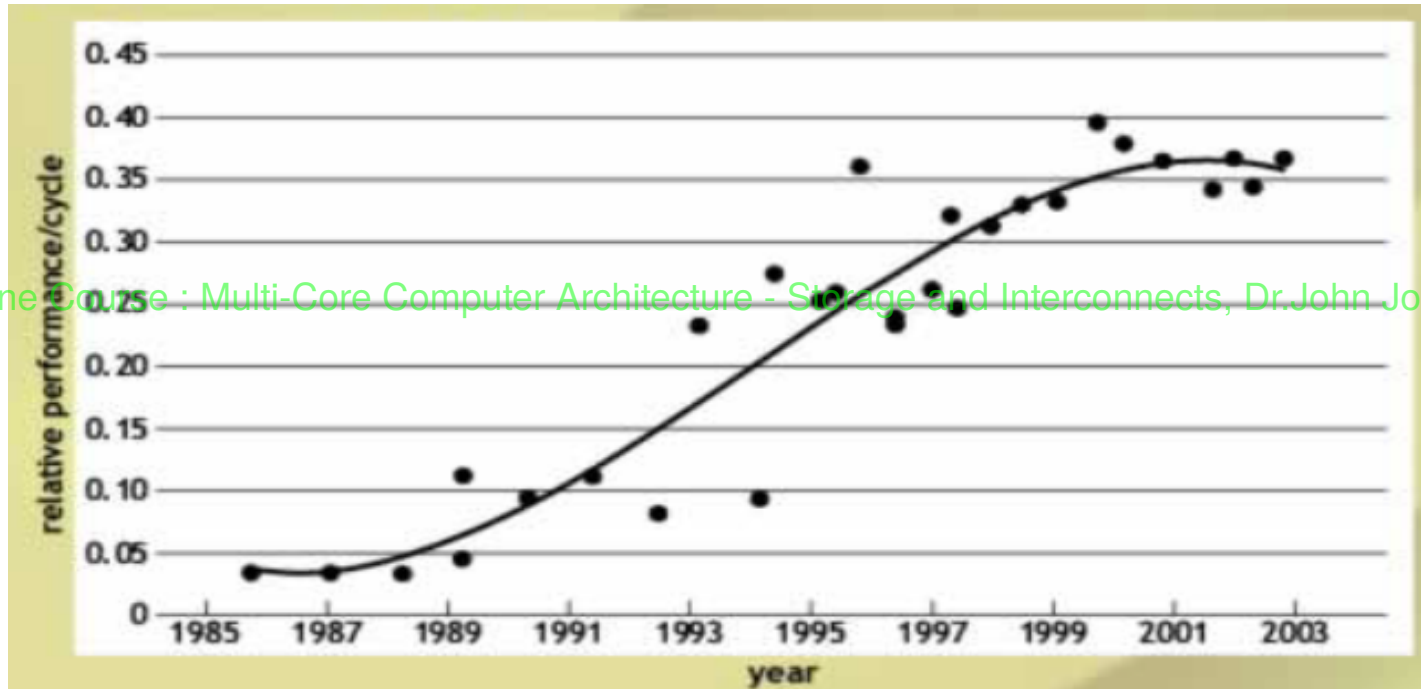
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Power Wall



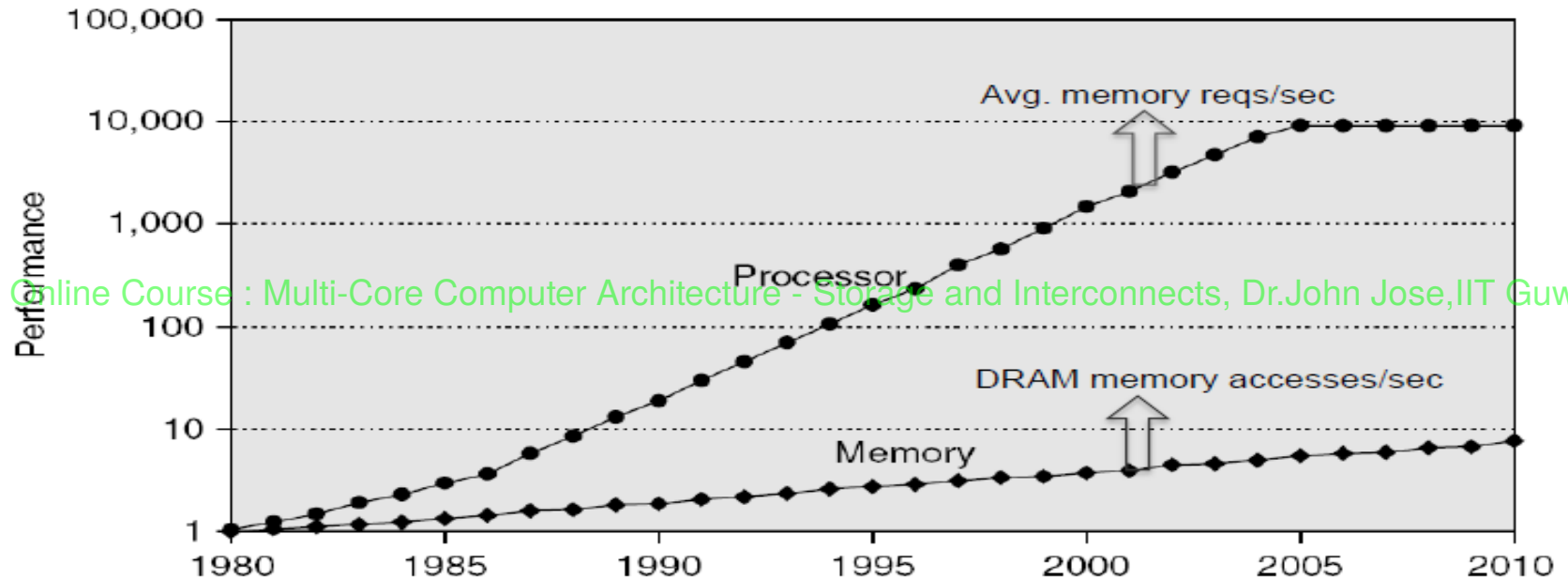
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ILP Wall



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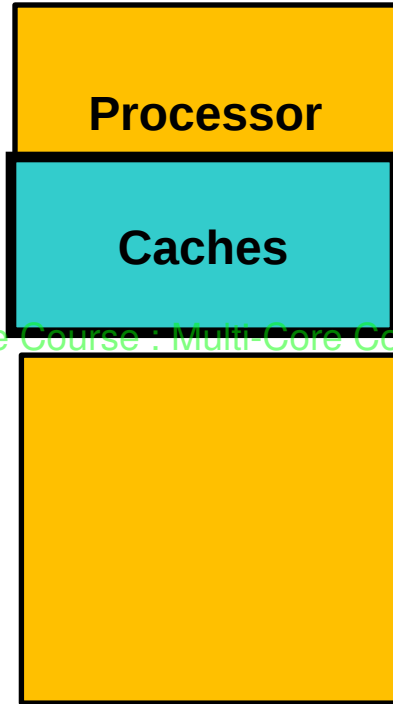
Memory Wall



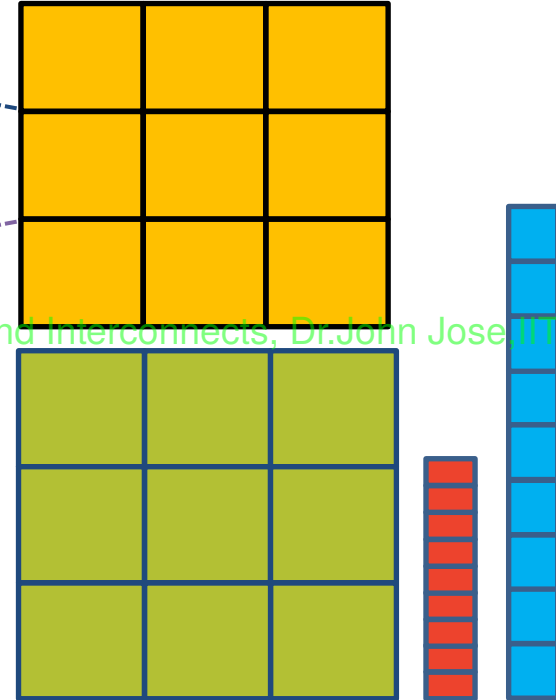
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Paradigm Shift to Multicore

2004 SoC : 90 nm



2017 SoC : 10 nm



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Multiple slower processors vs single fast powerful processor

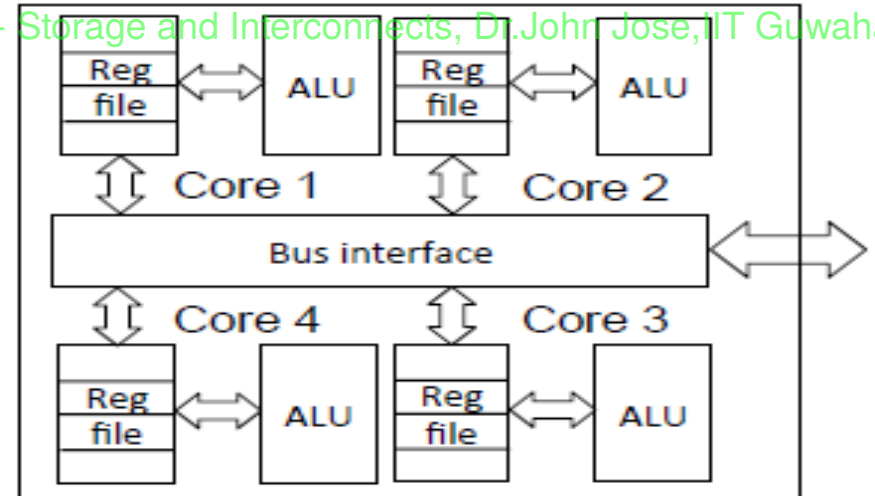
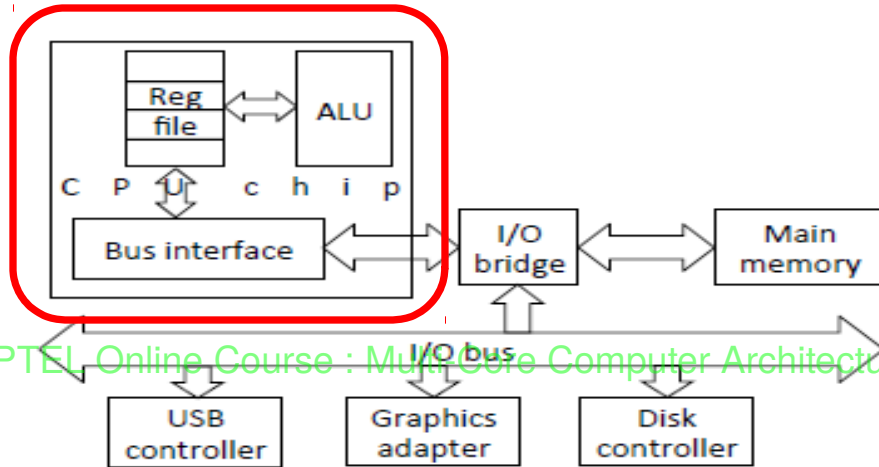
Paradigm Shift to Multicore



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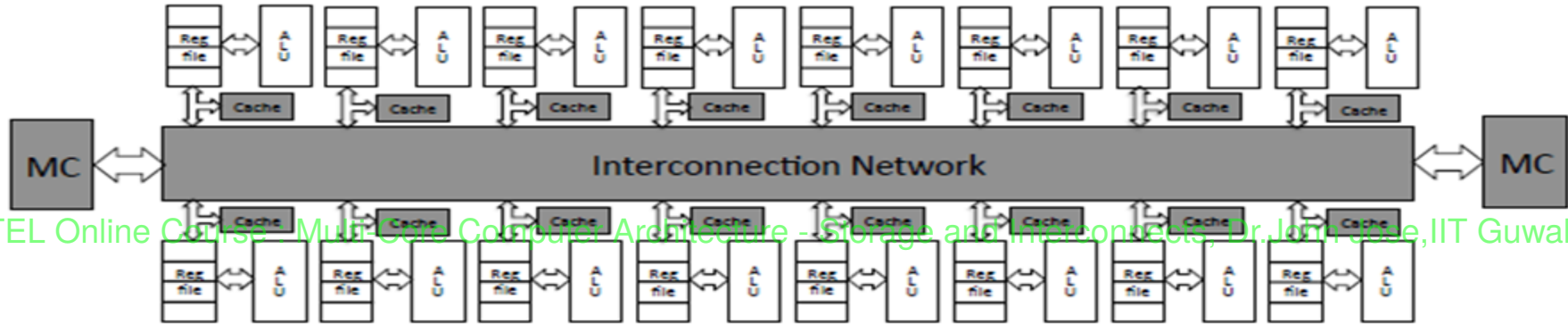
Multiple slower processors is better than single fast powerful processor

What is Multicore ?



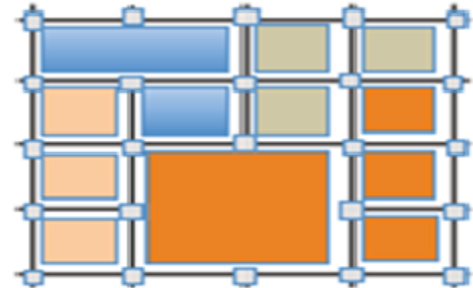
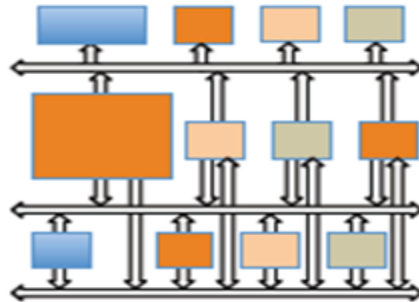
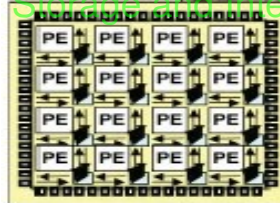
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What is Multicore ?

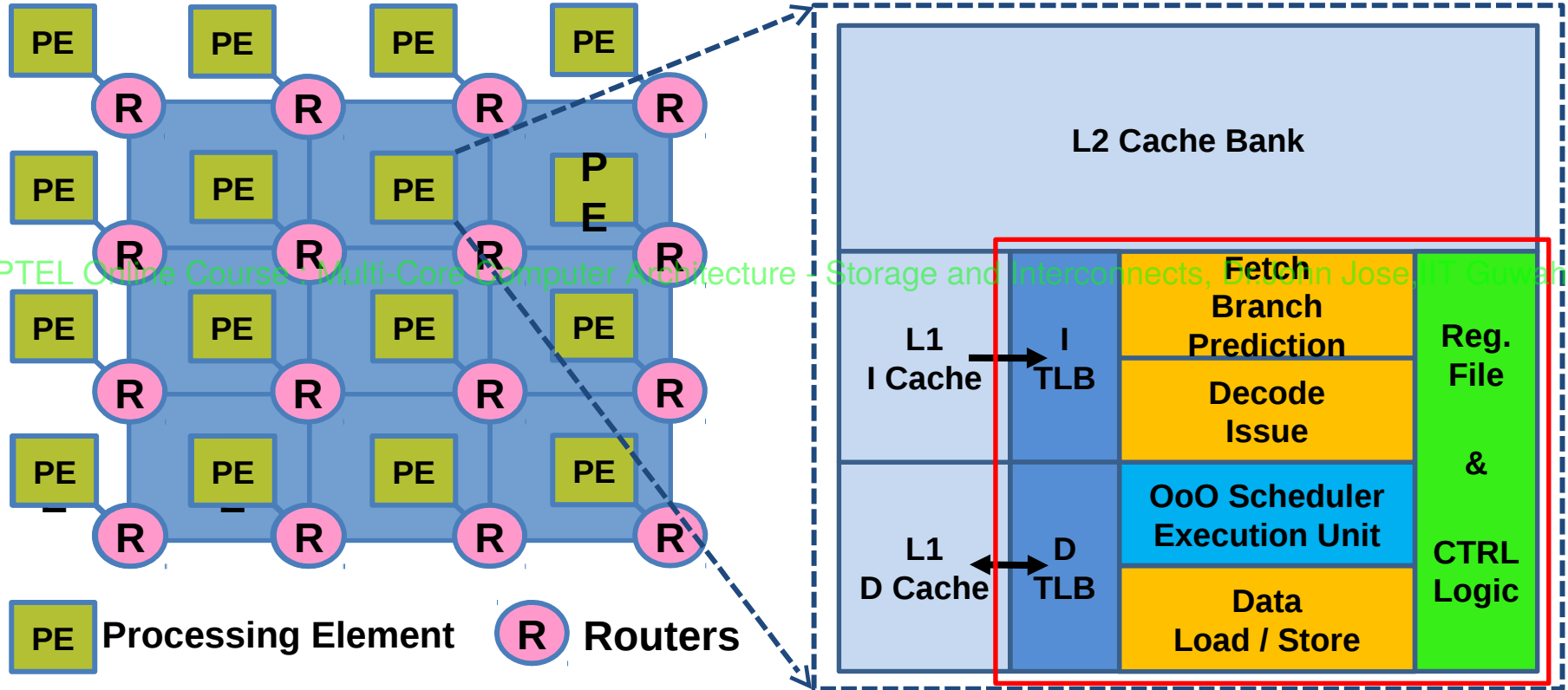


- ❖ How these cores communicate ?
- ❖ What is the best interconnection mechanism ?

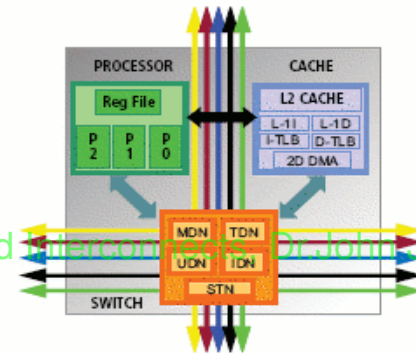
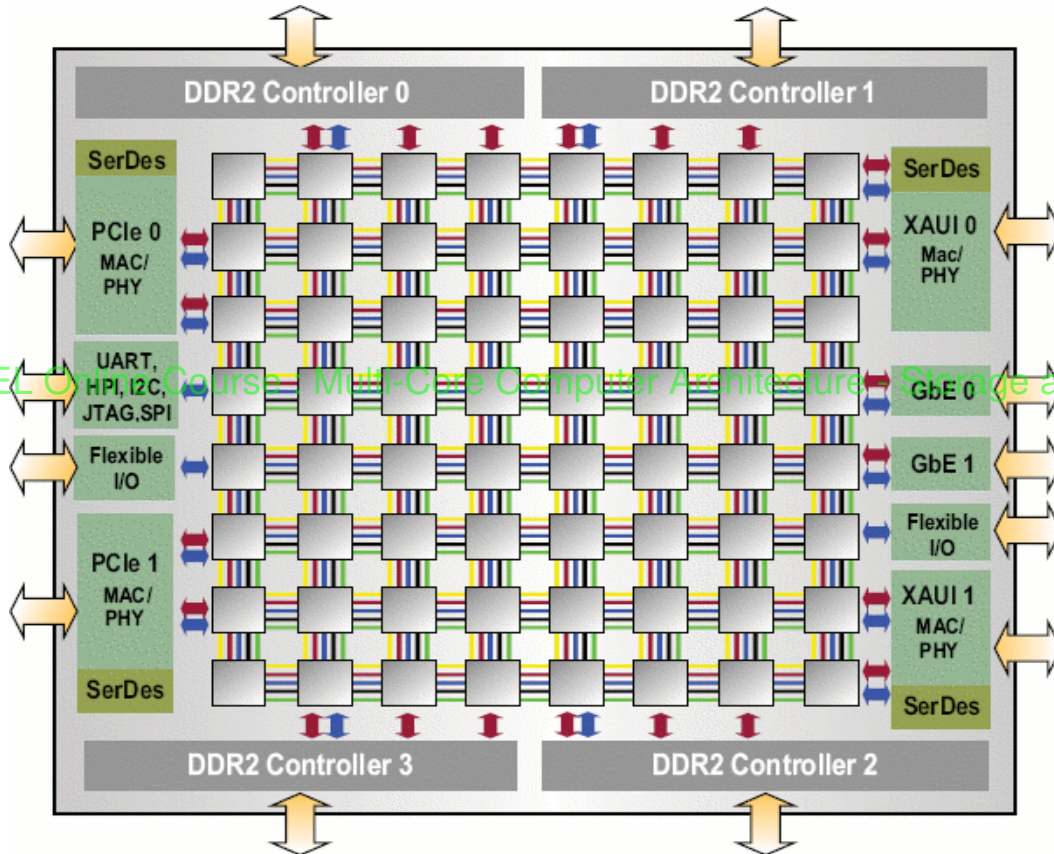
The Paradigm Shift



Tiled Chip Many-Core Processor (TCMP)

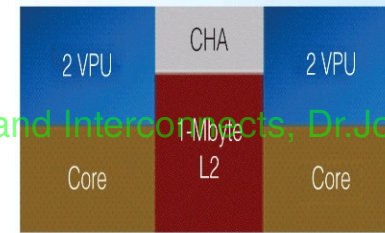
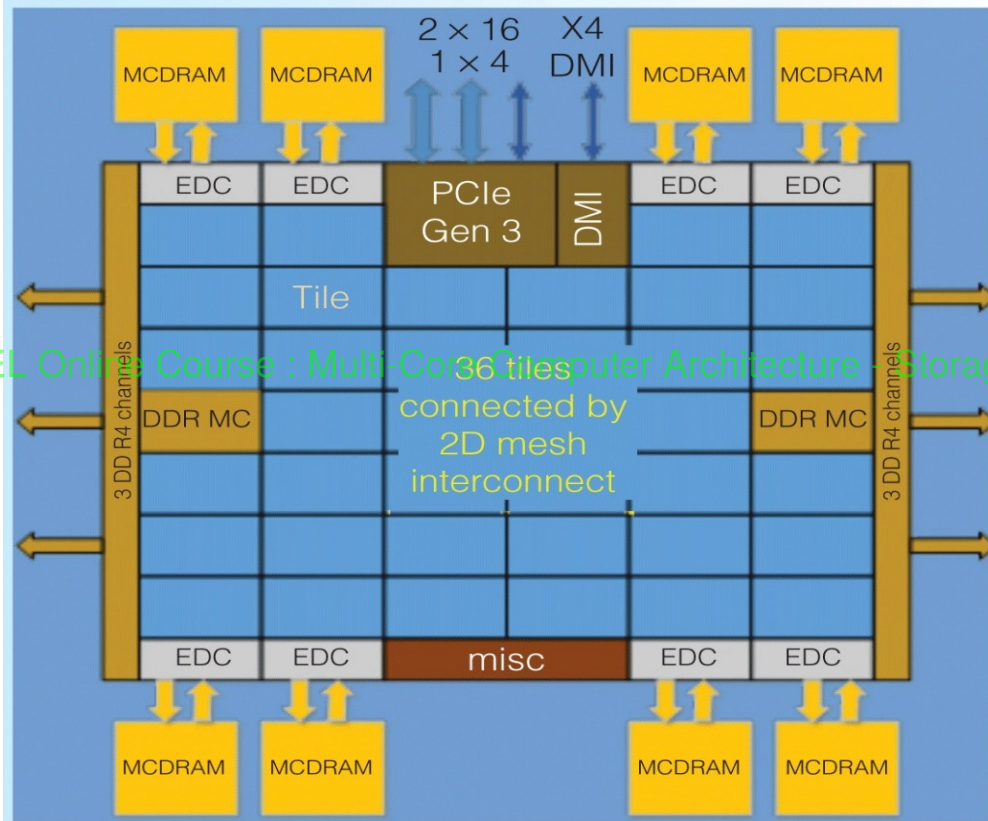


State-of-the-Art Architectures



Tiler64

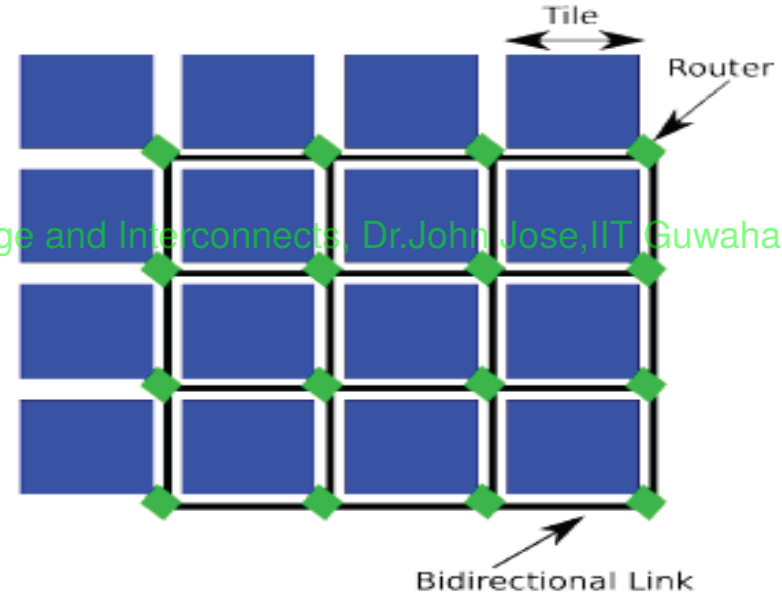
State-of-the-Art Architectures



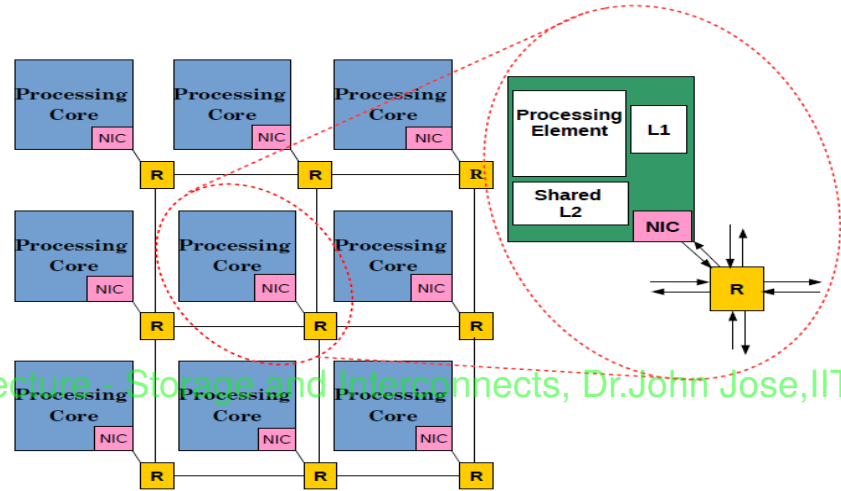
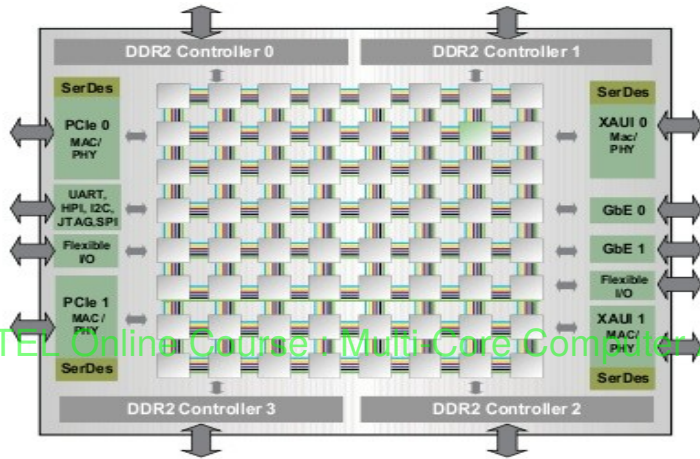
Intel KNL

What is NoC ?

- ❖ Processing units interconnected via packet based network
- ❖ Each resource is called as a **'tile'**
- ❖ All resources organized as rectangular tiles on the chip.
- ❖ Each tile have an address - (X,Y)
- ❖ Tiles interconnected by network of routers
- ❖ Communication by packet transmission

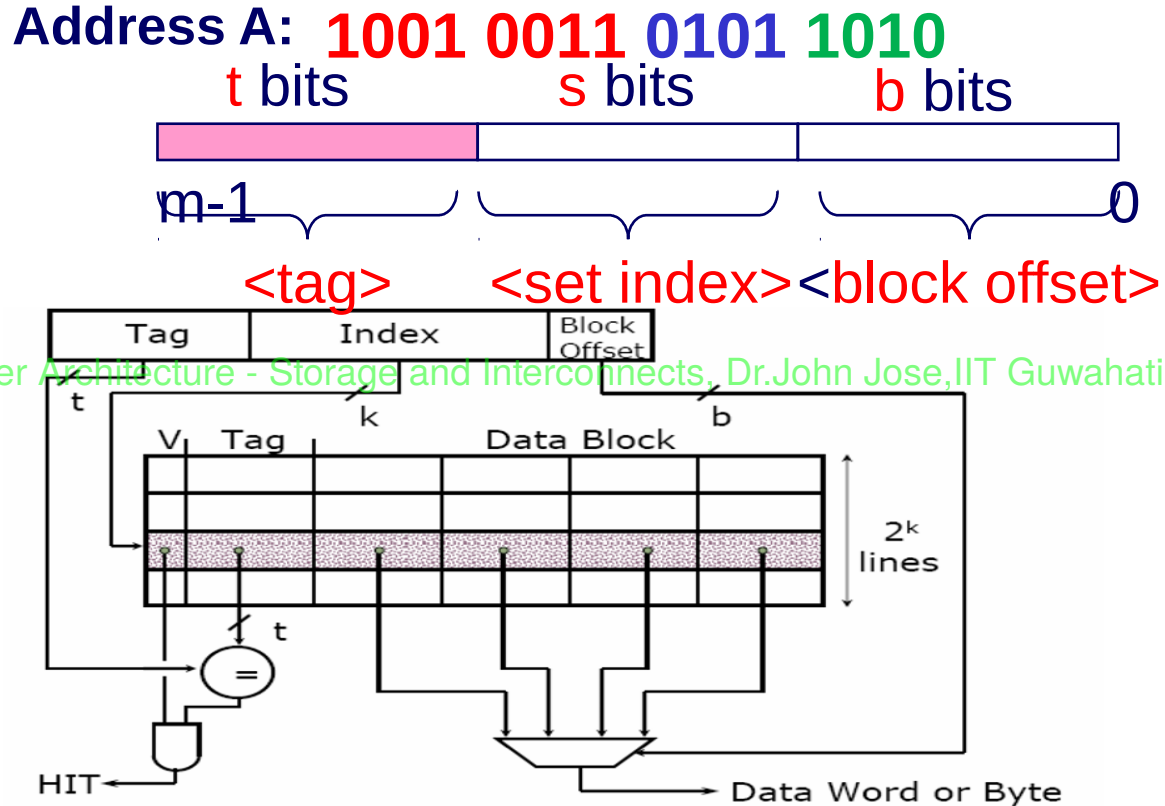
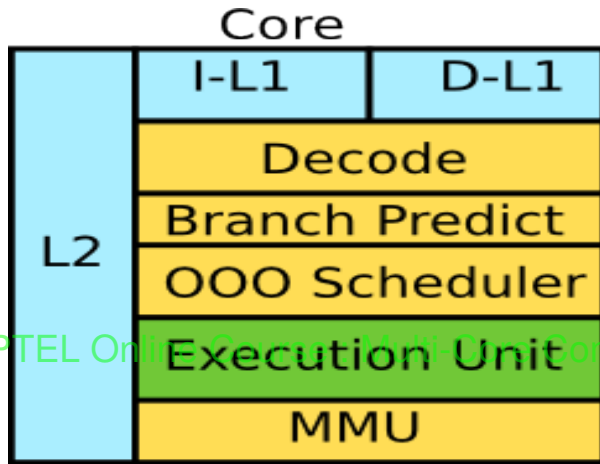


Routers and Tiles

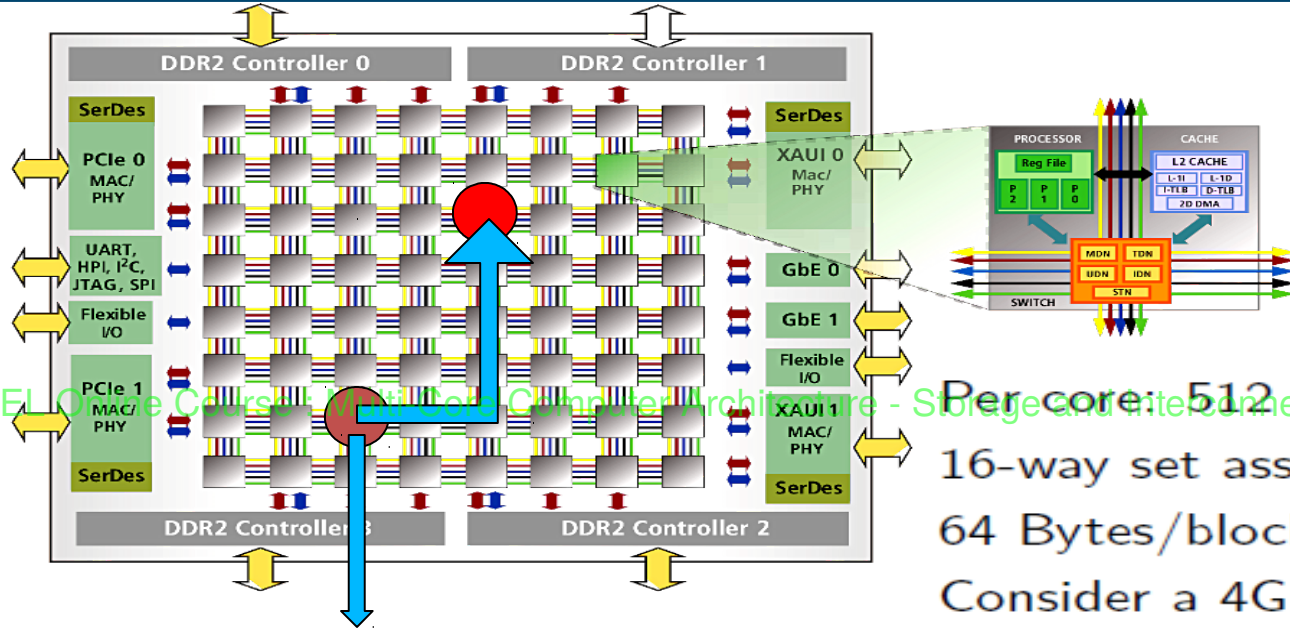


- ❖ East, West, North and South neighbors
- ❖ Packets are divided into flow control units called flits
- ❖ L1 and L2 cache misses create NoC traffic packets

What is the role of on-chip cache ?



On-Chip Cache Address Mapping



Per core: 512 KB

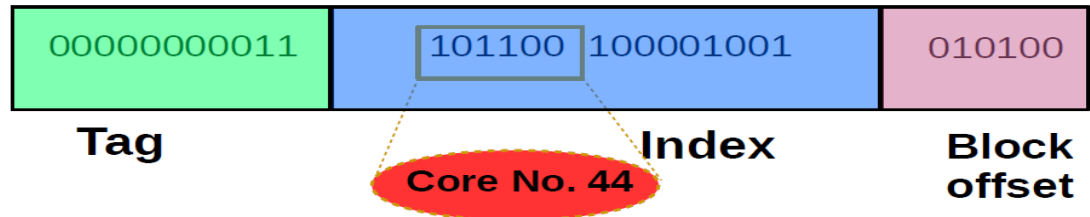
16-way set associative mapping

64 Bytes/block

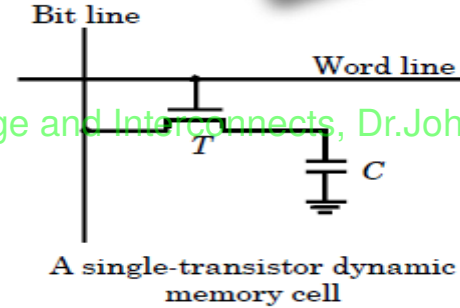
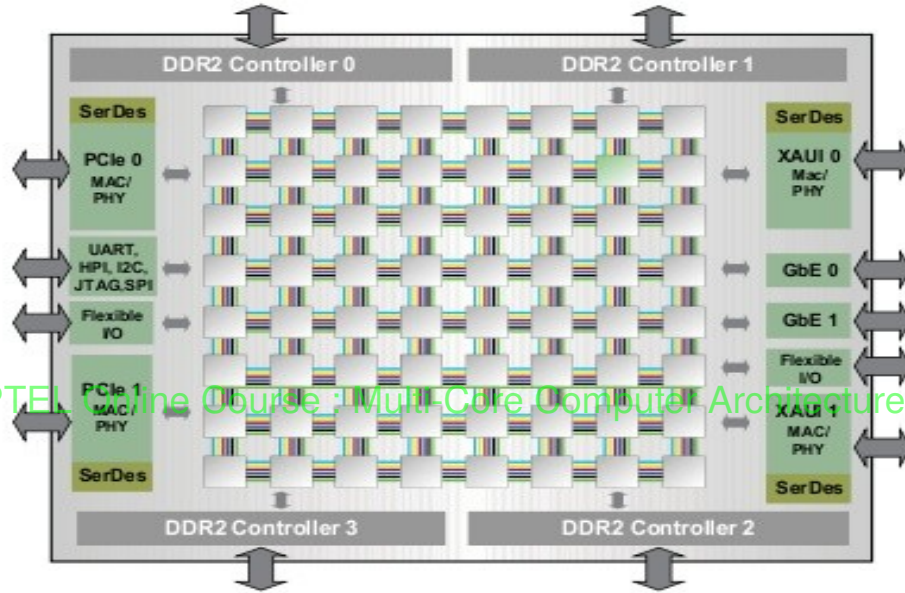
Consider a 4GB RAM (2^{32} bits)

Hex Address : 0x764254

11 bits	15 bits	6 bits
Tag	Index	Block offset



What is the role of memory controllers?



Packets & Flits

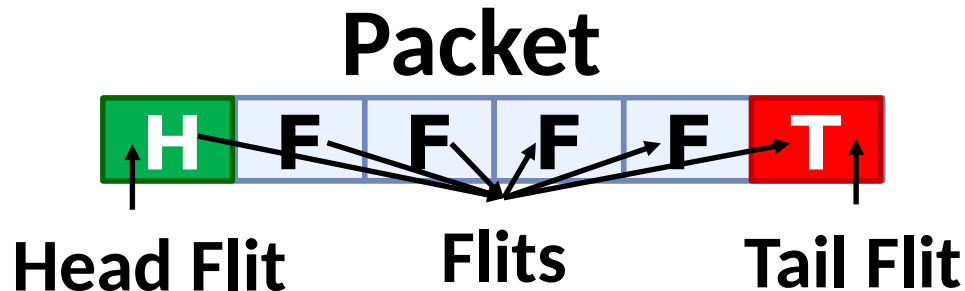
❖ Packet

- ❖ Unit of transfer for network

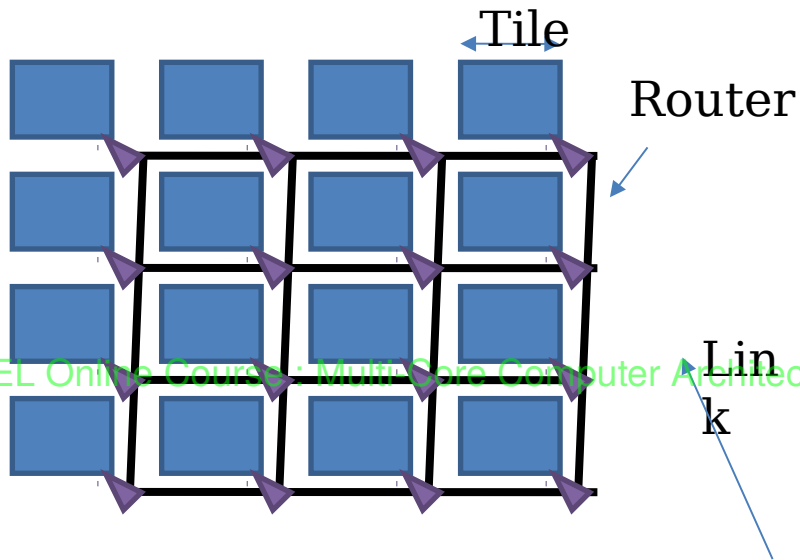
❖ Flit

- ❖ Basic unit of transfer between a pair of routers
- ❖ Unit of flow control within network

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Building Blocks of NoC



❖ **Topology**

❖ **Routing**

❖ **Flow control**

❖ **Router micro-architecture**

Building Blocks of NoC

- ❖ **Topology**

- ❖ Specifies the way switches are wired

- ❖ **Routing (algorithm)**

- ❖ How does a message move from source to destination

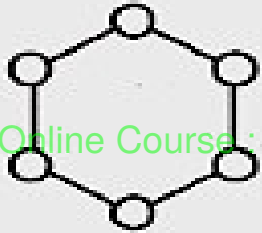
- ❖ **Buffering and Flow Control**

- ❖ What do we store within the network?

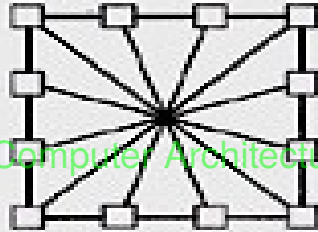
- ❖ Entire packets, parts of packets, etc?
 - ❖ What is basic unit of transfer

Topology

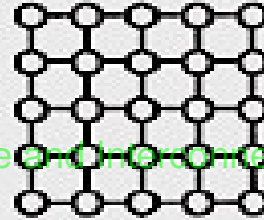
- ❖ Determines the physical layout and connection pattern between nodes and channels in the network.



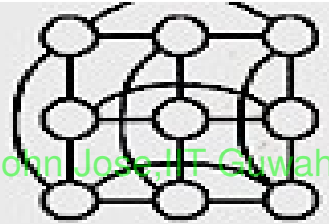
Ring



Spidergon



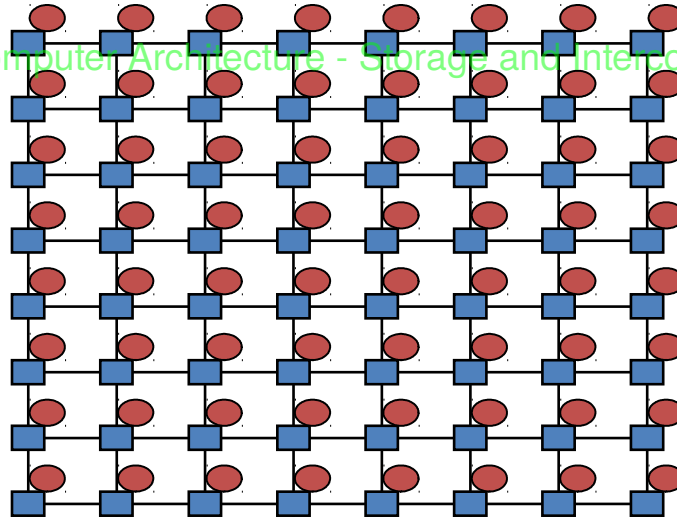
2D-mesh



2D-torus

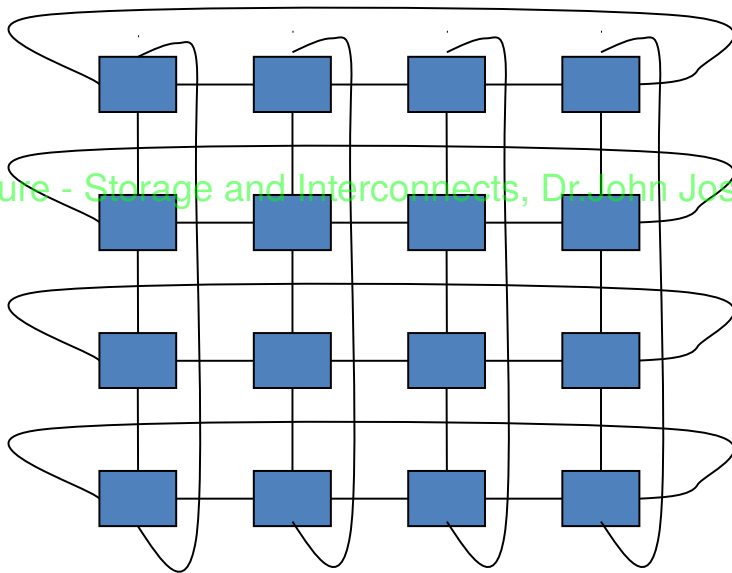
Mesh

- ❖ Each node connected to 4 neighbors (N, E, S, W)
- ❖ Easy to layout on-chip: regular and equal-length links
- ❖ Path diversity: many ways to get from one node to another



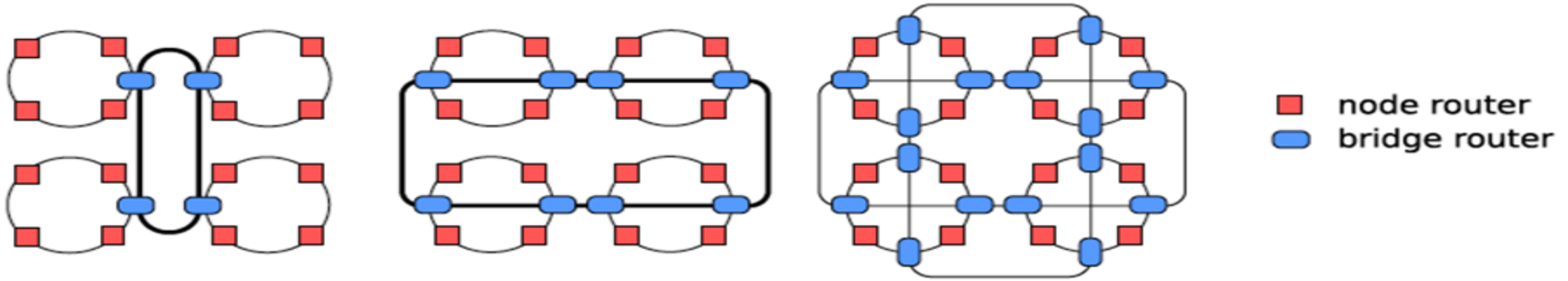
Torus

- ❖ Mesh is not symmetric on edges: performance very sensitive to placement of task on edge vs. middle
- ❖ Torus avoids this problem
- ❖ Harder to lay out on-chip
- ❖ Unequal link lengths



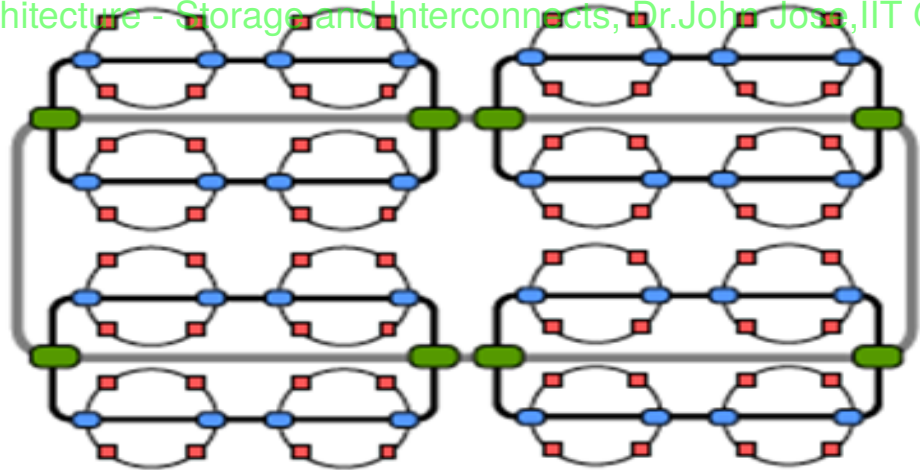
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Hierarchical Rings



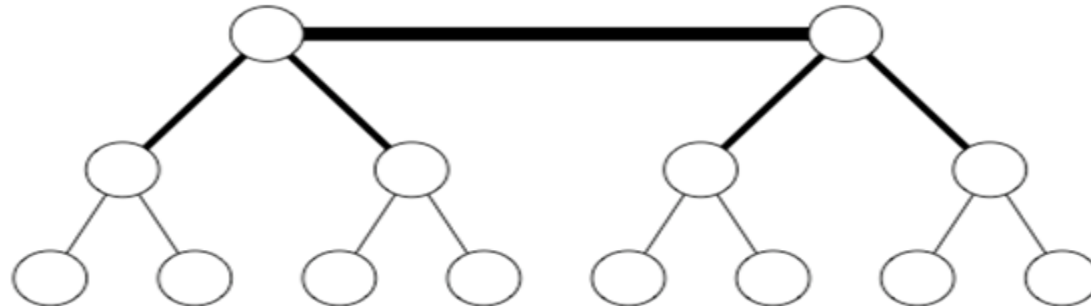
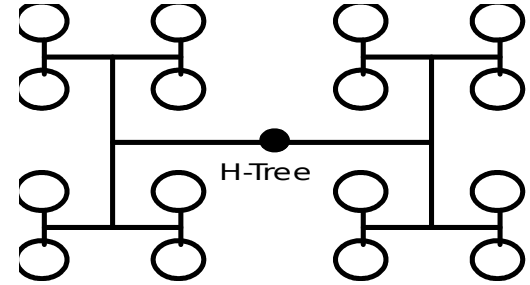
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- ❖ More scalable
- ❖ Lower latency
- ❖ More complex



Trees

- ❖ Planar, hierarchical topology
- ❖ Good for local traffic
- ❖ Easy to Layout
- ❖ Root can become a bottleneck
- ❖ Fat trees avoid this problem (CM-5)



Fat Tree

**THANK
YOU!**

**FOR
YOUR
PRESENCE**

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